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10/062,426	02/05/2002	Tae Yamane	OKI.302	4137

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/062,426	YAMANE, TAE	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3* is/are allowed.

6)☒ Claim(s) *5-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 10/09/2003 has been approved by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto (US Pat. 5289036) in view of Takao et al. (Japanese Pat. 2000-183214) and Yamaji et al. (US Pat. 6198165).

Regarding claims 5 and 7, Nishimoto discloses a resin sealed chip package/chip-size package (CSP), the CSP comprising:

- a semiconductor chip (101 in Fig. 1A/1B)

- electrodes/regions having gate and source/drain connections being formed on the chip (see connecting portions C1/104, C2 and C3 Fig. 1A; Col. 3, line 60- Col. 4, line 10)
- an insulating film/wafer coat (107 in Fig. 1A/1B) formed over the chip
- conductive wiring patterns (108B-1/108B-2/108C, etc. in Fig. 1A and 3 respectively) being formed on the insulating film/wafer coat, the metal electrode/pad being electrically connected to the wiring pattern (Col. 4, lines 1-10; Col. 5, lines 22-40)
- a molding resin (111 in Fig. 1B) being formed over the conductive wiring patterns
- conductive pads/metal posts (CP-109B and 209A in Fig. 1A and 3 respectively; Col. 4, line 4; Col. 5, line 28) being formed in the molding resin
- the conductive wiring patterns (CWP) being shaped/patterned to have a connecting portion between the CWP and the CP (not numerically referenced- see conductive region extending outwardly in a longitudinal direction from the conductive pads/metal posts and connecting 108C and 108B-1 in Fig. 1A), and
- terminals such as ground, power, etc. (not numerically referenced in Fig. 1A; Col. 4, line 20; Col. 5, line 29) being formed connecting the wiring pattern

(Fig. 1A/1B and 3; Col. 2, line 25- Col. 5, lines 22-48).

Nishimoto fails to:

a) explicitly show in a cross-sectional view of Fig. 1A/1B, the metal pad on the chip and the conductive post in the resin being connected with the terminal formed on the molding resin, and

b) teach a dummy pattern comprising two parts being arranged adjacent along sides/two sides of the connecting portion.

a) Takao et al. teach a conventional CSP having a chip with a metal/aluminum pad (52 in Fig. 11) where a conductive post (CP 55 in Fig. 11) formed in a resin (54 in Fig. 11) is connected to a terminal/bump (56 in Fig.11) on the resin (see Prior art description in English Translation, page 1 of 1).

b) Yamaji et al. teach a CSP having a number of dummy wiring patterns having a variety of configurations where the dummy wiring patterns having two regions/parts being arranged (see a layout of patterns 14 having large and small patterned areas on left side of the connecting portion and CP and large patterned area on right side of the same in Fig. 2; Col. 6, line 14- Col. 7, line 35) adjacent along two/both sides of a connecting portion (not numerically referenced- see connecting portion between 8 and 10 in Fig, 2) between a conductive wiring pattern and an external connecting electrode/conductive

post (8 and 10 respectively in Fig. 2) to improve the planarization and adhesion of an insulating layer and to minimize associated defects (Col. 7, lines 1- 35). Yamaji et al. further teach the two regions/parts being arranged (see the layout of 14 with respect to 8 in Fig. 2) along the conductive wiring pattern.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the conductive post being formed in the resin and the terminal being formed on the molding resin being connected as taught by Takao et al. and the dummy pattern arranged adjacent along both sides of the connecting portion and along the conductive wiring pattern as taught by Yamaji et al. so that the electrical testing, rework capability and adhesion of the insulating layer can be improved and the defect level can be reduced in Nishimoto's CSP.

Regarding claim 6, forming the dummy pattern during a same process as the conductive wiring pattern and arranging parallel to the same do not distinguish over Nishimoto, Takao et al. and Yamaji et al., because only the final product/structure is relevant, not the process or the sequence of forming and arranging the dummy pattern such as "before/after depositing the conductive pattern" or "during sputtering or any other process step". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ

324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

4. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto (US Pat. 5289036) in view of Takao et al. (Japanese Pat. 2000-183214) and Bertolet et al. (US Pat. 5844317).

Regarding claim 9, Nishimoto discloses a resin sealed chip package/chip-size package (CSP), the CSP comprising:

- a semiconductor chip (101 in Fig. 1A/1B)
- electrodes/regions having gate and source/drain connections being formed on the chip (see connecting portions C1/104, C2 and C3 Fig. 1A; Col. 3, line 60-Col. 4, line 10)
- an insulating film/wafer coat (107 in Fig. 1A/1B) formed over the chip

- conductive wiring patterns (108B-1/108B-2/108-3/108Bb and 208A-1/208A-2 in Fig. 1A and 3 respectively) being formed on the insulating film/wafer coat, the metal electrode/pad being electrically connected to the wiring pattern (Col. 4, lines 1-10; Col. 5, lines 22-40)
- a molding resin (111 in Fig. 1B) being formed over the conductive wiring patterns
- conductive pads/metal posts (109B and 209A in Fig. 1A and 3 respectively; Col. 4, line 4; Col. 5, line 28) being formed in the molding resin
- the conductive wiring patterns (CWP) being shaped/patterned to have a connecting portion between the CWP and the CP (not numerically referenced- see conductive region extending outwardly in a longitudinal direction from the conductive pads/metal posts and connecting 108C and 108B-1 in Fig. 1A), and
- terminals such as ground, power, etc. (not numerically referenced in Fig. 1A; Col. 4, line 20; Col. 5, line 29) being formed connecting the wiring pattern

(Fig. 1A/1B and 3; Col. 2, line 25- Col. 5, lines 22-48).

Nishimoto further discloses using recesses/dents in the conducting wiring pattern to provide the thinning of the wiring pattern (Col. 5, line 61).

Nishimoto fails to:

a) explicitly show in a cross-sectional view of Fig. 1A/1B, the metal pad on the chip and the conductive post in the resin being connected with the terminal formed on the molding resin, and

b) teach a dent being formed at and around the connecting portion.

a) Takao et al. teach a conventional CSP having a chip with a metal/aluminum pad (52 in Fig. 11) where a conductive post (55 in Fig. 11) formed in a resin (54 in Fig. 11) is connected to a terminal/bump (56 in Fig.11) on the resin (see Prior art description in English Translation).

b) Bertolet et al. teach a CSP having a metallization/conductive pattern including a conductive post/bump (CP) and a metallization/wiring pattern (20 and 28 respectively in Fig. 1 and 2) where a conductive strap/connecting portion is formed between the CP and the metallization/wiring pattern (see 16 in Fig. 1) to provide an improved adhesion and bonding strength for the metallization structure (Col. 8, lines 10-42), the metallization pattern further comprising a recess/dent (30 in Fig. 1 and 2) at/around the conductive strap/connecting portion (16 and 20 respectively in Fig. 1 and 2; Col. 7, line 25- Col. 8, line 42).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the conductive post being formed in the resin and the terminal being formed on the molding resin being connected as taught by Takao et al. and at least one of the conducting wiring pattern and the dent being formed at and around the connecting portion as taught by Bertolet et al. so that the cracking/delamination defects in the wiring layer can be reduced and the insulation coverage of the wiring layer, adhesion/bonding strength and an electrical testing/rework capability can be improved in Nishimoto's CSP.

Regarding claim 10, Nishimoto, Takao et al. and Bertolet et al. teach substantially the entire claimed structure as applied to claim 9 above, except the dent being a square shaped.

Bertolet et al. further teach the recess having length/width dimensions being such that the recess/dent has a rectangular shape (30 in Fig. 1) or selecting the width being higher or lower such that the recess/dent can be formed having a square or a rectangular shape (Col. 8, lines 27-33).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the dent being shaped to be a square as taught by Bertolet et al. so that the insulation coverage of the wiring layer can be improved and the photo/etch processing can be simplified in Nishimoto's CSP.

5. Claim 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto (US Pat. 5289036) in view of Takao et al. (Japanese Pat. 2000-183214) and Galloway (US Pat. 5886414).

Regarding claim 12, Nishimoto discloses a resin sealed chip package/chip-size package (CSP), the CSP comprising:

- a semiconductor chip (101 in Fig. 1A/1B)
- electrodes/regions having gate and source/drain connections being formed on the chip (see connecting portions C1/104, C2 and C3 Fig. 1A; Col. 3, line 60-Col. 4, line 10)
- an insulating film/wafer coat (107 in Fig. 1A/1B) formed over the chip
- conductive wiring patterns (108B-1/B-2,108C and 108A-1/A-2 in Fig. 1A) being formed on the insulating film/wafer coat, the metal electrode/pad being electrically connected to the wiring pattern (Col. 4, line 1-10)
- a molding resin (111 in Fig. 1B) being formed over the conductive wiring patterns
- conductive pads/metal posts (CP-109B, 109C, etc. in Fig. 1A; Col. 4, line 4) being formed in the molding resin
- the conductive wiring patterns (CWP) being shaped/patterned to have a connecting portion between the CWP and the CP (not numerically referenced-see conductive region extending outwardly in a longitudinal direction from the conductive pads/metal posts and connecting 108C and 108B-1 in Fig. 1A)

having a first region extending outwardly from the CP (see the region between 109C and 108C in Fig. 1A), and

- terminals such as ground, power, etc. (not numerically referenced in Fig. 1A; Col. 4, line 20) being formed connecting the wiring pattern

(Fig. 1A/1B; Col. 2, line 25- Col. 5, line 22).

Nishimoto fails to:

a) explicitly show in a cross-sectional view of Fig. 1A/1B the metal pad on the chip and the conductive post in the resin being connected with the terminal formed on the molding resin, and

b) teach the connecting portion having a second region extending in a perpendicular direction from the first region.

a) Takao et al. teach a conventional CSP having a chip with a metal/aluminum pad (52 in Fig. 11) where a conductive post (55 in Fig. 11) formed in a resin (54 in Fig. 11) is connected to a terminal/bump (56 in Fig.11) on the resin (see Prior art description in English Translation, page 1 of 1).

b) Galloway teaches a CSP having a metal pad and wiring pattern having a connecting portion to provide an extension regions for the wiring pattern where the

connecting portions have a variety of configurations including first and second regions (see 62 and a portion of 60 adjacent to 62 in Fig. 6B-7; Col. 2-4). Furthermore, such configurations include the first region extending outwardly (62 in Fig. 6A-7) and the second regions extending perpendicularly from both sides from the first region (see pattern in Fig. 6B showing the extension of the connecting portion in the perpendicular direction to provide further connection with the wiring 60) or obliquely (see Fig. 6C) from the first region (Col. 4, lines 37- 46).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the conductive post being formed in the resin and the terminal being formed on the molding resin being connected as taught by Takao et al. and the connecting portion having a second region extending in a perpendicular direction from the first region as taught by Galloway so that an electrical testing and rework capability can be improved in Nishimoto's CSP.

Regarding claims 13 and 14, Nishimoto, Takao et al. and Galloway teach substantially the entire claimed structure as applied to claim 12 above, including the second regions extending in a perpendicular direction from both sides of the first region, wherein Nishimoto further teaches the second region comprising a plurality of projecting parts/branched sections (108Ba, 108Bb, etc. in Fig. 1A), each extending in a perpendicular/lateral direction from the first region (Col. 4, line 36-50).

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto (US Pat. 5289036), Takao et al. (Japanese Pat. 2000-183214) and Yamaji et al. (US Pat. 6198165), as applied to claims 5 and 7 above, and further in view of Ogawa et al. (US Pat. 6237218).

Regarding claim 8, Nishimoto, Takao et al. and Yamaji et al. teach substantially the entire claimed structure as applied to claims 5 and 7 above, except the connecting portion having a width that decreases gradually from the conductive post to the conductive wiring pattern.

Ogawa et al. teach using a wiring substrate having a conductive wiring pattern/shape such that a connecting portion has a dimension/width that gradually decreases from a mid/central portion of a conductive pad/circular post (see 21a/21b/21c/21d and respective wiring layer 21 in Fig. 2B and 1) to a narrow/linear portion of the conductive wiring pattern (21 in Fig. 2B; Col. 12, line 55- Col. 13, line 13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the connecting portion having a width that decreases gradually from the conductive post to the conductive wiring pattern as taught by Ogawa et al. so that the insulation cracking and stress related defects can be reduced in Yamaji et al., Takao et al. and Nishimoto's CSP.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto (US Pat. 5289036), Takao et al. (Japanese Pat. 2000-183214) and Bertolet et al. (US Pat. 5844317), as applied to claim 9 above, and further in view of Ogawa et al. (US Pat. 6237218).

Regarding claim 11 Nishimoto, Takao et al. and Bertolet et al. teach substantially the entire claimed structure as applied to claim 10 above, except the connecting portion the connecting portion having a width that decreases gradually from the conductive post to the conductive wiring pattern.

Ogawa et al. teach using a wiring substrate having a conductive wiring pattern/shape such that a connecting portion has a dimension/width that gradually decreases from a mid/central portion of a conductive pad/circular post (see 21a/21b/21c/21d and respective wiring layer 21 in Fig. 2B and 1) to a narrow/linear portion of the conductive wiring pattern (21 in Fig. 2B; Col. 12, line 55- Col. 13, line 13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the connecting portion having a width that decreases gradually from the conductive post to the conductive wiring pattern as taught by Ogawa et al. so that the insulation cracking and stress related defects can be reduced in Bertolet et al., Takao et al and Nishimoto's CSP.

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto (US Pat. 5289036),Takao et al. (Japanese Pat. 2000-183214) and Galloway (US Pat. 5886414) as applied to claim 12 above, and further in view of Ogawa et al. (US Pat. 6237218).

Regarding claim 15, Nishimoto, Takao et al. and Galloway teach substantially the entire claimed structure as applied to claim 12 above, except the connecting portion having a width that decreases gradually from the conductive post to the conductive wiring pattern.

Ogawa et al. teach using a wiring substrate having a conductive wiring pattern/shape such that a width of a connecting portion gradually decreases from a mid/central portion of the conductive pad/circular post (see 21a/21b/21c/21d and respective wiring layer 21 in Fig. 2B and 1) to a narrow/linear portion of the conductive wiring pattern (21 in Fig. 2B; Col. 12, line 55- Col. 13, line 13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the connecting portion having the width that decreases gradually from the conductive post to the conductive wiring pattern as taught by Ogawa et al. so that the insulation cracking and stress related defects can be reduced in Galloway, Takao et al. and Nishimoto's CSP.

Response to Arguments

9. Applicant's arguments with respect to claims 5-8 and 12-16 have been considered but are moot in view of the new ground(s) of rejection.

10. Claims 9-11:

Applicant contends that Bertolet et al. teaches forming the aperture (13 in Fig. 1 and 2) in the passivation layer under the wiring layer and not the dent formed at and around the connecting portion as claimed.

However, as explained above, Bertolet et al. teach the conductive strap/connecting portion being formed between the CP and the metallization/wiring pattern (see 16 in Fig. 1). Such metallization structure further clearly shows the recess/dent (see 30 in Fig. 1 and 2) at/around the conductive strap/connecting portion (16 and 20 respectively in Fig. 1 and 2; Col. 7, line 25- Col. 8, line 42). Forming the aperture in the insulating layer is a process/method step used prior to forming the metallization structure and the same relates to the method of forming such structure.

Allowable Subject Matter

11. Claims 1-3 are allowed.

Reasons for Allowance

12. The following is an examiner's statement of reasons for allowance:

The references of record do not teach either singularly or in combination at least the limitations "the connecting portion having a width that gradually decreases toward the conductive wiring pattern, the connecting portion having a slit to disperse stress to be applied to the connecting portion" in a chip size semiconductor package having a connecting portion between the wiring pattern and a conductive post where the conductive post being formed in a molding resin.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference c is cited as being related to a CSP having a pad and a conductive wiring pattern.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP
01-29-04

EDDIE LEE
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